ECE 4214: Semiconductor Device Fundamentals
VIRGINIA TECH
Course Syllabus (CRN *12975)*
Spring 2018 TR 9:30-10:45 AM

I.   ECE 4214 SEMICONDUCTOR DEVICE FUNDAMENTALS

Instructor: Prof. Mantu Hudait, Dept. of ECE, 626 Whittemore Hall
Phone: 540-231-6663   Email: mantu.hudait@vt.edu

Class Room:	**SURGE 109**		
Final Exam date and time	Exam Date: **May 8th, 2018**	**Midterm-I (in class)**	**March 1st**
	Begin Time: 10:05 AM	**Midterm-II (in class)**	**April 5th**
	End Time: 12:05 PM	**Final (in class room)**	**May 8th**

Office Hours: **Tuesday**: 1:00-2:30pm and by appointment (e-mail please).

Course Description:

The course will cover the device physics and device applications: Fundamental semiconductor device physics associated with semiconductor devices and in-depth understanding of p/n junction diodes, bipolar junction transistors, MOS capacitor, and junction field effect transistors.

Learning Objectives:

Having successfully completed 4214, students will be able to:
- Determine the band structure of semiconductors when supplied with basic materials properties and applying their knowledge of quantum mechanics.
- Calculate carrier distributions in thermal equilibrium and non-thermal equilibrium conditions for intrinsic and doped semiconductors.
- Apply basic semiconductor drift-diffusion equations to determine current flow in semiconductor devices.
- Differentiate between the fundamental difference of p/n junctions and field effect transistors
- Determine alignment of metal-semiconductor band diagrams and identify whether junction is Ohmic or Schottky.
- Design a bipolar transistor, metal-oxide-semiconductor and/or a field effect transistor that meet specific performance criteria through the selection of the appropriate semiconductor material(s), doping, and device dimensions.

II.   PREREQUSITES & COREQUISITES

Prerequisites: 2204 or MSE 3204 or PHYS 3455.

The student will be introduced briefly the fundamentals of quantum mechanics. But some prior knowledge of this topic and solid-state physics will also help.

III. TEXTS AND SPECIAL TEACHING AIDS

Required Text

D.A. Neamen, *Semiconductor Physics & Devices*, 4th ed., McGraw-Hill, 2012; Hardcover, 768 pages©2012, ISBN-13 978-0-07-352958-5.

Additional Reference Books:

- Umesh Mishra and Jasprit Singh, *Semiconductor Device Physics and Design*, Springer, 2008 (e-book available through www.lib.vt.edu)
- M. Shur, *Physics of Semiconductor Devices*, Englewood Cliffs, NJ: Prentice Hall, 1990.
- J. Singh, *Semiconductor Devices: Basic Principles*, New York, NY: Wiley, 2001.
- B.G. Streetman and S. Bhattacharya, *Solid State Electronic Devices*, 4th ed., Englewood Cliffs, NJ: Prentice Hall, 1995.
- Robert Pierret, "Semiconductor Device Fundamentals", 1st or 2nd ed. [1996, Addison-Wesley or 2002, McGraw-Hill]

IV. EDUCATIONAL OBJECTIVES

The lecture sessions provides learning opportunities that should enable you to do the following upon completion of this course:

A. Develop a basic understanding on the following key concepts in quantum and statistical mechanics relevant to physical properties of electronic materials and their device applications:

i. Quantum Mechanics:

Crystal structure of solids; space lattices; wave particle duality; Schrodinger's wave equation; particle trapped in a box; particle tunneling through a barrier; allowed and forbidden energy bands; propagating electron wave in a periodic lattice; effective mass; density of states; strain effect on band structure; quantization effects in nanoscale devices

ii. Statistical Mechanics:

The Fermi-Dirac and Maxwell-Boltzmann probability distribution function; the Fermi energy;

iii. Equilibrium vs non-equilibrium properties:

Carrier distribution at equilibrium; doped semiconductors; compensated semiconductor; carrier transport phenomena; hall effect; excess carriers in semiconductors; continuity equation; Poisson's equation.

iv. p-n junction:

Carrier distribution and field profile at a p-n junction; diode I-V characteristics and non-idealities, diode capacitance, heterostructures, band alignment; quantum well properties.

v. MOS capacitors and field effect transistors:

Understand and interpret C-V characteristics; understand the physical structure and detailed operation of Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs); understand the terminal I-V characteristics of MOSFETs and their associated non-idealities due to scaling; high electron mobility transistors; tunnel transistors; FinFETs.

vi. Bipolar junction transistors:

Understand the physical operation of solar cell and its efficiency limits; heterojunctions to improve efficiency; potential impact on global energy crisis and light emitting diodes.

B. Become proficient with the fundamental device physics concepts

C. Learn to analyze device characteristics in detail and brainstorm ways towards improving them or adapting them to new applications

V.   SYLLABUS

Section 1

Topic	Number of Lectures (**Tentative**)
1. Crystalline Structures	2
2. Basic Quantum Mechanics and Bandgaps	2
3. Band Diagrams	1
4. Carrier Concentration and Fermi Level	3
5. Drift-diffusion and Carrier Mobility	2
6. Recombination and Generation of Carriers	2
7. Measurement of Resistivity and Mobility	Reading Materials
8. Midterm Exam 1	

Section 2

1. p-n Diodes	3
2. Schottky Diodes and Ohmic Contacts	1
3. Heterostructures	2
4. Bipolar Transistors	3
5. Midterm Exam 2	

Section 3

1. Field Effect Transistors, FinFETs	3
2. Tunnel FETs	2
3. Final Exam (<u>cover all chapters</u>)	

VI.   GRADING POLICY

Homework	**1%**
Pop-up test (based on assigned homework)	**9%**
Class Attendance	**5%**
Midterm-I	**20%**
Midterm-II	**25%**
Final (<u>all chapters</u>)	**40%**
Total	**100%**

<u>Home Work (Please Read): (1%)</u>

Homework problems will be typically be assigned on a weekly basis and will be due at the end of class one week following its assignment. <u>Homework may be turned in one day late with a 25% deduction</u>. **No assignments will be accepted until the solution is posted,** except in the case of unforeseen, <u>officially documented</u> absences.

Each problem solution should be **neatly worked out**. If a given assignment requires multiple pages of work, it must be stapled together prior to submission. Use neatly trimmed 8.5" x 11" paper and write on one side only. When possible, sketch illustrative diagrams and <u>label current, voltage, and other relevant quantities on the diagrams</u>. Very rough sketches with no labels will receive no credit. Use industrially accepted notation for units, per discussion on Day 1 of class.

<u>I will collect ALL assigned problems for grading</u>. *However, all problems may not necessarily be graded*. I expect you to have worked ALL the problems and to be prepared to submit the problem solutions in the above format <u>at the end of class on the date due</u>.

You may consult with other students and with your instructor while you are working on assigned problems but your goal in consulting should be limited to exploring options and approaches rather than avoiding work. The ability to solve problems develops through disciplined effort and the exams will require you to be able to solve problems. To obtain full credit for a homework assignment you must submit it to your instructor in class on the due date. Note that if you use open source solution for your homework, you will have a difficulty to answer questions in either midterm or final exam.

In-Class Activities (Please read): (9%)

There will be regular activities assigned during class (pop-up test) based on your homework, which will require your participation and may result in a submission at the end of the class period or within 5 min beginning of class. I will grade on these tests. These activities should help strengthen your understanding of the course materials and assist in preparing you for the exams and 9% is assigned for this activities. I usually ask questions during class and your participation is most important.

Attendance (Please read): (5%)

Attendance all lecture classes is expected and critical to your successfully completing the requirements of this course. I will periodically check attendance against the class roll and you will have only 3 missing classes due to unforeseen, <u>officially documented</u> absences without any penalties. However, chronic absenteeism will be noted, and I will not be inclined to give such individuals the benefit of the doubt in judgment situations such as borderline final grades. In the event that you miss a lecture, it is <u>your responsibility</u> to ask one of your classmates or read text book. If you have a conflict with a scheduled exam, you must make arrangements with your instructor well in advance so that alternate times can be scheduled.

Exams (Please read): (85% = 20%+25%+40%)

There will be only 2 mid-term exams and one final exam (March 1st for Midterm-I; April 5th Midterm-II; May 8th Final all in class room Surge 109). **No make-up exams will be given** except for unforeseen, <u>officially documented</u> absences. If such a circumstance arises on a test date, it is your responsibility to contact me as soon as possible. If you expect to be absent on a test date for any legitimate reason (conferences, job interviews, project team competitions, etc.), it is your responsibility to give me sufficient prior notice so that we can make other arrangements. There will be a **FINAL exam** at the end of this course (**Cumulative**).

VII. ACADEMIC INTEGRITY

The Virginia Tech Honor Code establishes the standard for **ACADEMIC INTEGRITY** in this course, and will be strictly enforced. *Discussion* of class material with your classmates or the instructor is encouraged; however, ALL submitted work, must represent your own efforts, and you must pledge to this effect on all work. For more details on the relevant honor codes, consult the websites listed below:

o   Undergraduate Honor System, http://www.honorsystem.vt.edu/index.html

The Undergraduate Honor Code pledge that each member of the university community agrees to abide by states:

"As a Hokie, I will conduct myself with honor and integrity at all times. I will not lie, cheat, or steal, nor will I accept the actions of those who do."

Students enrolled in this course are responsible for abiding by the Honor Code. A student who has doubts about how the Honor Code applies to any assignment is responsible for obtaining specific guidance from the course instructor before submitting the assignment for evaluation. Ignorance of the rules does not exclude any member of the University community from the requirements and expectations of the Honor Code. For additional information about the Honor Code, please visit:

- https://www.honorsystem.vt.edu/
- All assignments submitted shall be considered "graded work" and all aspects of your coursework are covered by the Honor Code. All projects and homework assignments are to be completed individually unless otherwise specified.
- Commission of any of the following acts shall constitute academic misconduct. This listing is not, however, exclusive of other acts that may reasonably be said to constitute academic misconduct. Clarification is provided for each definition with some examples of prohibited behaviors in the Undergraduate Honor Code Manual located at https://www.honorsystem.vt.edu/

A. CHEATING
- Cheating includes the intentional use of unauthorized materials, information, notes, study aids or other devices or materials in any academic exercise, or attempts thereof.

B. PLAGIARISM
- Plagiarism includes the copying of the language, structure, programming, computer code, ideas, and/or thoughts of another and passing off the same as one's own original work, or attempts thereof.

C. FALSIFICATION
- Falsification includes the statement of any untruth, either verbally or in writing, with respect to any element of one's academic work, or attempts thereof.

D. FABRICATION
- Fabrication includes making up data and results, and recording or reporting them, or submitting fabricated documents, or attempts thereof.

E. MULTIPLE SUBMISSION
- Multiple submission involves the submission for credit—without authorization of the instructor receiving the work—of substantial portions of any work (including oral reports) previously submitted for credit at any academic institution, or attempts thereof.

F. COMPLICITY
- Complicity includes intentionally helping another to engage in an act of academic misconduct, or attempts thereof.

G. VIOLATION OF UNIVERSITY, COLLEGE, DEPARTMENTAL, PROGRAM, COURSE, OR FACULTY RULES

- The violation of any University, College, Departmental, Program, Course, or Faculty Rules relating to academic matters that may lead to an unfair academic advantage by the student violating the rule(s).

Academic Misconduct Sanctions:

"If you have questions or are unclear about what constitutes academic misconduct on an assignment, please speak with me. I take the Honor Code very seriously in this course. The normal sanction I will recommend for a violation of the Honor Code is an **F*** sanction as your final course grade. The F represents failure in the course. The "*****" is intended to identify a student who has failed to uphold the values of academic integrity at Virginia Tech. A student who receives a sanction of **F*** as their final course grade shall have it documented on their transcript with the notation "FAILURE DUE TO ACADEMIC HONOR CODE VIOLATION." You would be required to complete an education program administered by the Honor System in order to have the "*****" and notation "FAILURE DUE TO ACADEMIC HONOR CODE VIOLATION" removed from your transcript. The "F" however would be permanently on your transcript."

VIII.   ANNOUNCEMENTS

I will use Canvas to post homework assignments, homework solutions, and other information pertaining to the course materials. You should check your email and the Canvas on a regular basis. In case, I use any teaching materials not from the text book, I will post **only those lecture notes** in Canvas. Lecture notes I prepared for enhancement you participation in class. You need to read the text book prior to class or after the class, please!

Read Chapters for this course:

Chapter-1: pages 1-20 (exercise: 21-24)
Chapter-2: pages 25-52 (exercise: 52-57)
Chapter-3: pages 58-100 (exercise: 100-104)
Chapter-4: pages 106-149 (exercise: 149-154)
Chapter-5: pages 156-1840 (exercise: 184-191)
Chapter-6: pages 192-201 (exercise: 233-240)
Chapter-7: pages 241-262 (exercise: 269-274)
Chapter-8: pages 276-295 (exercise: 323-330)
Chapter-9: pages 331-364 (exercise: 365-370)
Chapter-10: pages 371-419 (exercise: 433-441)
Chapter-12: pages 491-521 (exercise: 560-565)
Chapter-14: if time permits